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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,032	05/28/2002	Horea-Stefan Culca	521.1014	7295
7278	7590	08/18/2006	EXAMINER	
DARBY & DARBY P.C. P. O. BOX 5257 NEW YORK, NY 10150-5257			ETTEHADIEH, ASLAN	
		ART UNIT	PAPER NUMBER	
		2611		

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,032	CULCA, HOREA-STEFAN	
	Examiner	Art Unit	
	Aslan Ettehadieh	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 23 June 2006.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 5-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 8,11 and 12 is/are allowed.

6) Claim(s) 5-7,9 and 10 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

 1. Certified copies of the priority documents have been received.

 2. Certified copies of the priority documents have been received in Application No. _____.

 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION***Response to Arguments***

1. Applicant's arguments with respect to claims 5 – 7 and 9 – 10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 5 – 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 6247082) in view of Bacigalupo et al. (US 6032178).
3. Regarding claim 5, Lo discloses a data transmission device (col. 4 lines 48 – 50) for serial (col. 1 line 30) synchronous (col. 2 line 32) data transmission comprising:

a master device including a first arithmetic unit (figure 2 element 100a) and a master interface (figure 2 element 110a); and

a slave device including a second arithmetic unit (figure 2 element 100b) and a slave interface (figure 2 element 110b); wherein:

at least one data transmission line (figure 2 element 150) and a clock signal line (figure 2 element 124);

the second arithmetic unit is capable of generating the acknowledgment signal upon completion of a data reading operation (col. 3 line 66 – col. 4 line 6); and

the first arithmetic unit is configured so that a capability of the master device to initiate a further write operation to the slave device is dependent upon a receiving of the acknowledgment signal from the slave device (col. 7 line 57 – col. 8 line 55; where the ready signal is also being interpreted as an acknowledgment signal). Lo does not disclose the master and slave interfaces are capable of being connected via at least one data transmission line and a clock signal line and the master and the slave interfaces are capable of being connected via a acknowledgment signal line configured for a transmission of an acknowledgment signal from the slave device to the master device.

In the same field of endeavor, however, Bacigalupo discloses the master and slave interfaces are capable of being connected via at least one data transmission line and a clock signal line (figure 1 elements 1, 2, 6, 7, col. 2 line 56 – col. 3 line 32; where the connections to elements 1 and 2 are being interpreted as interfaces, as in applicants drawing of figure 1 and applicant's specification, paragraph 14) and the master and the slave interfaces are capable of being connected via a acknowledgment signal line configured for a transmission of an acknowledgment signal from the slave device to the master device (figure 1 elements 1, 2, 13, col. 5 lines 11 – 20). Bacigalupo also discloses a capability of the master device to initiate a further write operation to the slave device is dependent upon a receiving of the acknowledgment signal from the slave device (col. 5 lines 33 – 48).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use the master and slave interfaces are capable of

being connected via at least one data transmission line and a clock signal line and the master and the slave interfaces are capable of being connected via a acknowledgment signal line configured for a transmission of an acknowledgment signal from the slave device to the master device as taught by Bacigalupo in the system of Lo to enable more flexible data transmission (col. 2 lines 10 – 26).

4. Regarding claim 6, Lo further discloses at least one data transmission line is a single bidirectional data transmission line (figure 2 element 150; where the single communication line shows directional arrows on both ends showing a bidirectional (two directional) type of transportation). Bacigalupo also further discloses at least one data transmission line is a single bidirectional data transmission line (col. 3 lines 13 – 15).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 6247082) in view of Bacigalupo et al. (US 6032178) in further view of Siu et al. (US 5528215).

6. Regarding claim 7, Lo discloses the at least one data transmission line includes a first and a second unidirectional data transmission line (col. 4 lines 53 – 55). Lo is silent about a unidirectional data transmission line. Bacigalupo does discloses a unidirectional address transmission line (col. 3 lines 15 – 16).

In the same field of endeavor, however, Siu discloses a unidirectional data transmission line (col. 6 lines 22 – 27).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a unidirectional data transmission line as taught by Siu in the system of Lo because bidirectional transmission lines use time to set

up the direction of transmission and are susceptible to data collision where unidirectional transmission provides for more efficient and reliable data transfer.

7. Claim 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 6247082) in view of Bacigalupo et al. (US 6032178) in further view of Gulick (US 6058443).

8. Regarding claim 9, Lo discloses the second arithmetic unit is configured to receive data of the data reading operation from the master device and to generate and send to the master device a receive signal (col. 3 lines 41 – 43). Lo does not disclose a receive bit as only a single bit after a receiving of the data.

In the same field of endeavor, however, Gulick discloses to generate and send a receive bit as only a single bit after a receiving of the data.

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use to generate and send a receive bit as only a single bit after a receiving of the data as taught by Gulick in the system of Lo to decrease information in the transmission to allow for more data to be transmitted thus providing for a lower bandwidth consumption and/or faster transmission speeds.

9. Regarding claim 10, Lo discloses the first arithmetic unit is configured to generate and send data of the data reading operation to the slave device as a signal (col. 3 lines 41 – 43). Lo does not disclose only a single transmit bit.

In the same field of endeavor, however, Gulick discloses generate and send data of the data reading operation as only a single transmit bit.

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use generate and send data of the data reading operation as only a single transmit bit as taught by Gulick in the system of Lo to decrease information in the transmission to allow for more data to be transmitted thus providing for a lower bandwidth consumption and/or faster transmission speeds.

Allowable Subject Matter

Claims 8 and 11 – 12 are allowed. The following is an examiner's statement of reasons for allowance:

A comprehensive search of prior art of record failed to teach, either alone or in combination, a method/apparatus for activating and deactivating in transmission of bits of data between master and slave devices comprising applying multiple interference suppression measures between master and slave devices and the master device receiving a second acknowledgement signal after a fifth slave-master transmission delay with initiating a last cycle using a master device by transmitting a last transmit bit; deactivating the clock signal and reading a receive bit of a previous cycle while applying a fifth interference suppression measure as recited in the independent claim 8 and in combination with other elements of the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aslan Ettehadieh whose telephone number is (571) 272-8729. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aslan Ettehadieh
Examiner
Art Unit 2637

AE



MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER